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09/634,552	08/08/2000	Ahmadreza Rofougaran	36601/CAG/B600	4410

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EXAMINER	
LY, NGHI H	

ART UNIT	PAPER NUMBER
2617	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/634,552	ROFOUGARAN ET AL.	
	Examiner	Art Unit	
	Nghi H. Ly	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,32-43,51-77,85-90,92-105,112-123 and 164* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,32-43,51-77,85-90,92-105,112-123 and 164* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-14, 19-21, 32-37, 42, 43, 51-77, 85-90, 92-95, 100-102, 112-118, 122, 123 and 164 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US 6,366,622) in view of Birlrson (US 6,714,776).

Regarding claims 1, 51, 66 and 85, Brown teaches a method of wireless communications using a transceiver having a receiver and transmitter (see Title, Abstract, fig.4 and fig.5), comprising: programming one of the receiver and the

transmitter to process communication protocol for a local area network or a personal area network (see column 4, lines 63-67, column 7, lines 3-13, column 7, lines 60-64, and column 2, lines 1-6, see “LAN”, and column 22, lines 2-8, see "local area networks (LAN)"), receiving a first signal at the receiver from a wireless source (see Title, Abstract, fig.4 and fig.5), and transmitting a second signal from the transmitter into space (see Title, Abstract, fig.4 and fig.5), wherein the programming comprises programming a demodulator with a demodulation (see Abstract, column 7, lines 2-21, column 8, lines 25-36, column 10, lines 16-31, column 13, lines 14-37, and column 23, lines 50-57, see “demodulate”, “demodulation”, “demodulator” and/or “demodulating”. In order for the demodulator of Brown to demodulate, those skilled in the art will appreciate that the demodulator of Brown has been programmed to do so. If not, as alleged by the applicant, the demodulator of Brown will not demodulate at all. In addition, the applicant’s specification fails to further define how a demodulator can be programmed).

Brown does not specifically disclose the receiver comprises a low intermediate frequency (IF) heterodyne architecture, wherein the transmitter, the receiver and a local oscillator (LO) are integrated on a single integrated circuit chip, wherein the LO comprises a voltage controlled oscillator (VCO), a frequency divider and a mixer, wherein an output of the VCO is operatively coupled to an input of the frequency divider and to an input of the mixer, wherein an output of frequency divider is operatively coupled to the input of the mixer, and wherein the output of the mixer is operatively coupled to a downconverter of the receiver that downconverts the received first signal

and to an upconverter of the transmitter, wherein the second signal has been upconverted by the upconverter of the transmitter.

Birleson teaches the receiver comprises a low intermediate frequency (IF) heterodyne architecture, wherein the transmitter, the receiver and a local oscillator (LO) are integrated on a single integrated circuit chip (see column 4, lines 60 to column 5, line 5), wherein the LO comprises a voltage controlled oscillator (VCO) (see column 5, lines 6-15), a frequency divider and a mixer (see Abstract and column 2, lines 29-46), wherein an output of the VCO is operatively coupled to an input of the frequency divider and to an input of the mixer (see column 5, lines 6-15 and see Abstract and column 2, lines 29-46), wherein an output of frequency divider is operatively coupled to the input of the mixer (see fig.2), and wherein the output of the mixer is operatively coupled to a downconverter of the receiver that downconverts the received first signal and to an upconverter of the transmitter (see fig.2 and column 9, lines 28-34), wherein the second signal has been upconverted by the upconverter of the transmitter (see fig.2 and column 9, lines 35-57).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide a system and method for a single conversion tuner which generally uses phase shifted in-phase and quadrature-phase signal paths as an image rejection circuit (see Birleson, Abstract).

Regarding claims 32 and 112, Brown teaches a method an apparatus for wireless communications using a receiver (see Title, Abstract, fig.4, fig.5, column 21, lines 52-55, column 23, line 1-6, see “transceiver” and “integrated circuit”), transmitter

and local oscillator (see column 4, lines 57-76, see “transmitter”, column 2, lines 39-44, column 7, lines 60-67 and column 8, lines 8-21, see “oscillator”), comprising: programming one of the receiver and the transmitter to process communication protocol for a local area network or personal area network (see column 2, lines 1-6 and column 22, lines 2-8, and see column 4, lines 63-67, column 7, lines 3-13, column 7, lines 60-64, column 2, lines 1-6, see “LAN”, and column 22, lines 2-8, see "local area networks (LAN)"), programming a frequency of a clock in the local oscillator (see column 35, lines 8-15 and column 29, line 61 to column 30, line 12), receiving a first signal at the receiver from a wireless source (see Title, Abstract, fig.4, fig.5, column 21, lines 52-55), downconverting the received first signal with the clock (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61, see “up-convert” and/or “down-convert”), upconverting a second signal with the clock (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61, see “up-convert” and/or “down-convert”), and transmitting the upconverted second signal from the transmitter into space (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61, see “up-convert” and/or “down-convert”), the programming comprises programming a demodulator with a demodulation (see Abstract, column 7, lines 2-21, column 8, lines 25-36, column 10, lines 16-31, column 13, lines 14-37, and column 23, lines 50-57, see “demodulate”, “demodulation”, “demodulator” and/or “demodulating”. In order for the demodulator of Brown to demodulate, those skilled in the art will appreciate that the demodulator of Brown has been programmed to do so. If not, as alleged by the

applicant, the demodulator of Brown will not demodulate at all. In addition, the applicant's specification fails to further define how a demodulator can be programmed).

Brown does not specifically disclose the receiver comprises a low intermediate frequency (IF) heterodyne architecture, wherein the transmitter, the receiver and the LO are integrated on a single integrated circuit chip, wherein the LO comprises a voltage controlled oscillator (VCO), a frequency divider and a mixer, wherein an output of the VCO is operatively coupled to an input of the frequency divider and to an input of the mixer, wherein an output of frequency divider is operatively coupled to the input of the mixer, and wherein the output of the mixer is operatively coupled to a downconverter of the receiver that downconverts the received first signal and to an upconverter of the transmitter that upconverts the second signal.

Birleson teaches the receiver comprises a low intermediate frequency (IF) heterodyne architecture, wherein the transmitter, the receiver and the LO are integrated on a single integrated circuit chip (see Abstract, column 4, lines 60 to column 5, line 5), wherein the LO comprises a voltage controlled oscillator (VCO) (see column 5, lines 6-15), a frequency divider and a mixer (see column 4, lines 60 to column 5, line 5), wherein an output of the VCO is operatively coupled to an input of the frequency divider and to an input of the mixer (see column 5, lines 6-15 and see Abstract and column 2, lines 29-46), wherein an output of frequency divider is operatively coupled to the input of the mixer (see fig.2 and column 9, lines 28-34), and wherein the output of the mixer is operatively coupled to a downconverter of the receiver that downconverts the received

first signal and to an upconverter of the transmitter that upconverts the second signal (see fig.2 and column 9, lines 35-57).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide a system and method for a single conversion tuner which generally uses phase shifted in-phase and quadrature-phase signal paths as an image rejection circuit (see Birleson, Abstract).

Regarding claims 2-10, 13, 33, 35-37, 42, 43, 52-58, 67-70, 86-90, 92-95, 113-117, 122 and 123, Brown further teaches the second signal has been filtered by a filter, and wherein the the programming comprises programming a frequency band of the filter and programming gain of the amplifier (see Title, Abstract, fig.4, fig.5).

Regarding claims 11, 12 and 59, Brown further teaches the second signal has been filtered by a second filter and amplified by a second amplifier, and wherein the programming comprises programming a frequency band of the second filter and programming a gain of the second amplifier (see Title, Abstract, fig.4, fig.5).

Regarding claims 14, 72 and 118, Brown teaches that the downconversion comprises mixing the first signal with a clock and that second clock is mixed with a third clock (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61).

Regarding claims 19, 20, 21 and 100-102, Brown teaches the second signal has been filtered by a programmable low pass filter before being transmitted (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61).

Regarding claim 34, the combination of Brown further teaches the received first signal is downconverted to an intermediate frequency signal (see column 8, lines 8-21, column 10, lines 16-31 and column 11, lines 49-61).

Regarding claims 60-65, Brown teaches the receiver comprises a multiple stage amplifier in which each stage of the amplifier is programmable (see column 2, lines 26-39, column 25, lines 11-15, column 2, lines 26-34 and column 10, lines 32-44).

Regarding claims 71, Brown further teaches the transmitter component comprises a second filter with a programmable frequency band that filters a baseband signal, wherein the upconverter comprises a fourth mixer coupled to the second filter that mixes the clock with the filtered baseband signal, and wherein the transmitter comprises a second amplifier coupled to the fourth mixer and having a programmable gain (see Abstract, column 2, lines 26-34 and column 10, lines 32-44).

Regarding claims 73-76, Brown further teaches the frequency divider having a control input coupled to the controller to program a frequency of the second clock (column 25, lines 10-15, column 10, lines 51-54 and column 11, lines 57-61 and see column 2, lines 45-49).

Regarding claim 77, Brown further teaches programmable phase lock loop is couple to the VCO (column 2, lines 26-30 and column 10, lines 51-54).

Regarding claim 164, Brown teaches the communication protocol is associated with at least **one of** HomeRF, IEEE 802.11 and/or Bluetooth (see column 3, lines 10-13, column 3, lines 25-29 and column 21, lines 24-42).

4. Claims 15, 38 and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US 6,366,622) in view of Birlrson (US 6,714,776) and further in view of Okada et al (US 5,787,123)

Regarding claims 15, 38 and 96, the combination of Brown and Birleson teaches claims 1, 51, 66 and 85. The combination of Brown and Birleson does not specifically disclose generating the clock by mixing a second clock with a third clock.

Okada teaches generating the clock by mixing a second clock with a third clock (see fig.4b, item 49).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Okada into the system of Borwn and Birleson in order to generate clock with higher accuracy (see Okada, Abstract).

5. Claims 16-18, 39-41 and 97-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US 6,366,622) in view of Birlrson (US 6,714,776) and further in view of Okada et al (US 5,787,123) and Chen et al (US 5,940,456).

Regarding claims 16, 39 and 97, the combination of Brown, Birleson and Okada teaches claims 1, 32, 51, 85 and 112. The combination of Brown, Birleson and Okada does not specifically disclose generating the third clock by dividing a frequency of the second clock by an integer N.

Chen teaches generating the third clock by dividing a frequency of the second clock by an integer N (see column 7, lines 26-30).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Chen into the system of Borwn, Birleson and Okada in order to allow multiple data streams to be transmitted from one point to another (see Chen, column 2, lines 39-42).

Regarding claims 17, 40 and 98, the combination of Brown, Birleson and Okada teaches claims 1, 32, 51, 85 and 112. The combination of Brown, Birleson and Okada does not specifically disclose generating the third clock by dividing the second clock by an integer N.

Chen teaches generating the third clock by dividing the second clock by an integer N (see column 7, lines 26-30).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Chen into the system of Borwn, Birleson and Okada in order to allow multiple data streams to be transmitted from one point to another (see Chen, column 2, lines 39-42).

Regarding claims 18, 41 and 99, the combination of Brown, Birleson and Okada teaches claims 1, 32, 51, 85 and 112. The combination of Brown, Birleson and Okada does not specifically disclose the clock comprises a frequency fLo equal to fvco (N+1)/N wherein fvco equals a frequency of the second clock where N=2.

Chen teaches the clock comprises a frequency fLo equal to fvco (N+1)/N wherein fvco equals a frequency of the second clock and where N=2 (see column 7, lines 26-30).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Chen into the system of Borwn, Birleson and Okada in order to allow multiple data streams to be transmitted from one point to another (see Chen, column 2, lines 39-42).

6. Claims 22-24, 103-105 and 119-121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (US 6,366,622) in view of Birlrson (US 6,714,776) and further in view of Chen et al (US 5,940,456).

Regarding claims 22, 103 and 119, the combination of Brown and Birleson teaches claims 1, 32, 51, 85 and 112. The combination of Brown and Birleson does not specifically disclose teaches claims 1, 32, 51, 85 and 112. Brown does not specifically disclose generating the third clock by dividing a frequency of the second clock by an integer N.

Chen teaches generating the third clock by dividing a frequency of the second clock by an integer N (see column 7, lines 26-30).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Chen into the system of Brown and Birleson in order to allow multiple data streams to be transmitted from one point to another (see Chen, column 2, lines 39-42).

Regarding claims 23, 24, 104, 105, 120 and 121, the combination of Brown and Birleson teaches claims 1, 32, 51, 85 and 112. The combination of Brown and Birleson

does not specifically disclose the clock comprises a frequency fLo equal to fvco (N+1)/N wherein fvco equals a frequency of the second clock where N=2.

Chen teaches the clock comprises a frequency fLo equal to fvco (N+1)/N wherein fvco equals a frequency of the second clock and where N=2 (see column 7, lines 26-30).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to provide the teaching of Chen into the system of Brown and Birleson in order to allow multiple data streams to be transmitted from one point to another (see Chen, column 2, lines 39-42).

Response to Arguments

7. Applicant's arguments with respect to claims 1-24, 32-43, 51-77, 85-90, 92-105, 112-123 and 164 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghi H. Ly whose telephone number is (571)272-7911. The examiner can normally be reached on 9:30am-8:00pm Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dwayne Bost can be reached on (571) 272-7023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghi H. Ly

/Nghi H. Ly/
Primary Examiner, Art Unit 2617